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S a r h T rms

1	CAPACITANCE
2	CAPACITANCES
3	COUPLING
4	COUPLINGS
5	CR SS
6	CROSS-TALK
7	CROSS-TALKS
8	CROSSES
9	DELAY
10	DELAYED
11	DELAYING
12	DELAYINGS
13	DELAYS
14	INTERCONNECT
15	INTERCONNECTS
16	PROPAGATED
17	PROPAGATING
18	PROPAGATINGS
19	PROPAGATION
20	PROPAGATIONS
21	SUBSTRATE
22	SUBSTRATES
23	TALK
24	TALKS
25	TEST
26	TESTED
27	TESTER

	Total	USPAT	US-PGPU B	EPO	JPO	Derwent	IBM TDB	USOCR
1	223175							
2	35488							
3	941761							
4	70025							
5	2345914							
6	15885							
7	205							
8	69253							
9	529282							
10	204684							
11	76016							
12	7							
13		124830						
14		169536						
15		89143						
16		73309						
17		62959						
18		1						
19		172726						
20		4068						
21		1526591						
22		326543						
23		43220						
24		2577						
25		999096						
26		450271						
27		81705						
								27

	S arch T rms
28	TESTERS
29	TESTING
30	TESTINGS
31	TESTS
32	((((INTERCONNECT SAME CAPACITANCE) AND (PROPAGATED OR PROPAGATING OR PROPAGATION) SAME (DELAYING OR DELAYED OR DELAY))) AND (COUPLING SAME SUBSTRATE)) AND (CROSS-TALK OR TALK OR CROSS)) AND (TESTER OR TESTED OR TESTING

	T	tal	USPAT	US-PGPU	EPO	JPO	Derwent	IBM TDB	US	CR
28		7196								
29		475252								
30		939								
31		375382								
		29								
		32								

	U	1	Document ID	Issu	Dat	Pag	Title	Current OR
1	<input type="checkbox"/>	<input type="checkbox"/> US A1	20030083840	20030501	20		Apparatus and method for determining effect of on-chip noise on signal propagation	702/117
2	<input checked="" type="checkbox"/>	<input type="checkbox"/> US A1	20020000669	20020103	8		DEVICE COMPRISING THERMALLY STABLE, LOW DIELECTRIC CONSTANT MATERIAL	257/759
3	<input checked="" type="checkbox"/>	<input type="checkbox"/> US 6499131 B1	20021224	17			Method for verification of crosstalk noise in a CMOS design	716/5
4	<input checked="" type="checkbox"/>	<input type="checkbox"/> US 6469390 B2	20021022				Device comprising thermally stable, low dielectric constant material	257/758
5	<input checked="" type="checkbox"/>	<input type="checkbox"/> US 6462998 B1	20021008				Programmable and electrically configurable latch timing circuit	365/205
6	<input checked="" type="checkbox"/>	<input type="checkbox"/> US 6462584 B1	20021008				GENERATING A TAIL CURRENT FOR A DIFFERENTIAL TRANSISTOR PAIR USING A CAPACITIVE DEVICE TO PROJECT A CURRENT FLOWING THROUGH A CURRENT SOURCE DEVICE ONTO A NODE HAVING A DIFFERENT VOLTAGE THAN THE CURRENT SOURCE DEVICE	327/52

	Curr nt	XR f	R tri val	Inv	ntor	S	C	P	2	3	4	5
1				Corr, William E.		☒	☐	☐	☐	☐	☐	☐
2	257/642; 257/758			CHANG, CHORNG-PING et al.		☐	☐	☐	☐	☐	☐	☐
3	716/6; 716/8			Savithri, Nagaraj N. et al.		☐	☐	☐	☐	☐	☐	☐
4	257/637; 257/642; 257/752; 257/759; 257/E23.144; 257/E23.167			Chang, Chorng-Ping et al.		☐	☐	☐	☐	☐	☐	☐
5	365/194; 365/201; 365/233			Proebsting, Robert J.		☐	☐	☐	☐	☐	☐	☐
6	365/203; 365/204			Proebsting, Robert J.		☐	☐	☐	☐	☐	☐	☐

	Image Doc. Displayed	PT
1	US 20030083840	<input type="checkbox"/>
2	US 20020000669	<input type="checkbox"/>
3	US 6499131	<input type="checkbox"/>
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U	1	Document ID	I su	Date	Page s	Title	Curr nt OR
7	<input checked="" type="checkbox"/>	<input type="checkbox"/> US 6442644 B1	200020827			Memory system having synchronous-link DRAM (SLDRAM) devices and controller	711/105
8	<input checked="" type="checkbox"/>	<input type="checkbox"/> US 6378109 B1	200020423			Method of simulation for gate oxide integrity check on an entire IC	716/4
9	<input checked="" type="checkbox"/>	<input type="checkbox"/> US 6373753 B1	200020416			Memory array having selected word lines driven to an internally-generated boosted voltage that is substantially independent of VDD	365/189.09
10	<input checked="" type="checkbox"/>	<input type="checkbox"/> US 6363516 B1	200020326			Method for hierarchical parasitic extraction of a CMOS design	716/5
11	<input checked="" type="checkbox"/>	<input type="checkbox"/> US 6356485 B1	200020312			Merging write cycles by comparing at least a portion of the respective write cycle addresses	365/189.01
12	<input checked="" type="checkbox"/>	<input type="checkbox"/> US 6333656 B1	200011225			Flip-flops	327/202
13	<input checked="" type="checkbox"/>	<input type="checkbox"/> US 6297668 B1	200011002			Serial device compaction for improving integrated circuit layouts	326/101
14	<input checked="" type="checkbox"/>	<input type="checkbox"/> US 6282135 B1	200010828			Intializing memory cells within a dynamic memory array prior to performing internal memory operations	365/203

	Curr nt	XR f	R tri val	Inv	ntor	S	C	P	2	3	4	5
7	365/194			Gustavson, David B. et al.		<input type="checkbox"/>						
8	716/2			Young, Duane J. et al.		<input type="checkbox"/>						
9			365/226; 365/230.06		Proebsting, Robert J.		<input type="checkbox"/>					
10			716/10; 716/13		Cano, Francisco A. et al.		<input type="checkbox"/>					
11			365/189.07; 365/222		Proebsting, Robert J.		<input type="checkbox"/>					
12			327/203		Schober, Robert C.		<input type="checkbox"/>					
13			326/102; 326/103		Schober, Robert C.		<input type="checkbox"/>					
14			365/149; 365/226		Proebsting, Robert J.		<input type="checkbox"/>					

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7	<input type="checkbox"/>
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	U	1	Docum nt ID	Issu Date	Pages	Title	Curr nt OR
15	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6253359 B1	20010626		Method for analyzing circuit delays caused by capacitive coupling in digital circuits	716/6
16	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6252448 B1	20010626		Coincident complementary clock generator for logic circuits	327/259
17	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6240046 B1	20010529		Integrated circuit random access memory capable of reading either one or more than one data word in a single clock cycle	365/233
18	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6212109 B1	20010403		Dynamic memory array having write data applied to selected bit line sense amplifiers before sensing to write associated selected memory cells	365/190
19	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6208575 B1	20010327		Dynamic memory array bit line sense amplifier enabled to drive toward, but stopped before substantially reaching, a source of voltage	365/208
20	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6198682 B1	20010306		Hierarchical dynamic memory array architecture using read amplifiers separate from bit line sense amplifiers	365/207
21	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6198324 B1	20010306		Flip flops	327/202

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15	716/5; 716/8		Cano, Francisco A. et al.	<input type="checkbox"/>						
16	327/256		Schober, Robert C.	<input type="checkbox"/>						
17	365/189.02; 365/189.05; 365/220; 365/226; 365/227; 365/230.03; 365/230.08		Proebsting, Robert J.	<input type="checkbox"/>						
18	365/189.01; 365/230.03		Proebsting, Robert J.	<input type="checkbox"/>						
19	365/207		Proebsting, Robert J.	<input type="checkbox"/>						
20	365/190		Proebsting, Robert J.	<input type="checkbox"/>						
21	327/217		Schober, Robert C.	<input type="checkbox"/>						

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15	<input type="checkbox"/>	
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20	<input type="checkbox"/>	
21	<input type="checkbox"/>	

	U	1	Docum nt ID	Issue Dat	Page s	Title	Curr nt OR
22	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6163475 A	200001219		Bit line cross-over layout arrangement	365/63
23	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6104653 A	200000815		Equilibration circuit and method using a pulsed equilibrate signal and a level equilibrate signal	365/203
24	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5880026 A	19990309		Method for air gap formation by plasma treatment of aluminum interconnects	438/688
25	<input checked="" type="checkbox"/>	<input type="checkbox"/>				Ultrathin electronics	438/455
26	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5610833 A	19970311		Computer-aided design methods and apparatus for multilevel interconnect technologies	716/11
27	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5121067 A	19920609		Directional sampling bridge	324/637

	Curr nt XRef	R tri val Classif	Inv ntor	S	C	P	2	3	4	5
22	365/51; 365/69	Proebsting, Robert J.		<input type="checkbox"/>						
23	365/190; 365/196; 365/202	Proebsting, Robert J.		<input type="checkbox"/>						
24	257/E21.581; 257/E23.144; 438/619; 438/671; 438/699	Xing, Guoqiang et al.		<input type="checkbox"/>						
25	257/E21.505; 257/E21.705; 438/458; 438/459; 438/7; 438/975; 438/977	Davidson, Howard L.		<input type="checkbox"/>						
26	257/E23.151; 716/15; 716/16	Chang, Norman H. et al.		<input type="checkbox"/>						
27	257/E27.012; 324/638; 324/648	Marsland, Robert A.		<input type="checkbox"/>						

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22		<input type="checkbox"/>
23	<input type="checkbox"/>	<input type="checkbox"/>
24		<input type="checkbox"/>
25		<input type="checkbox"/>
26		<input type="checkbox"/>
27		<input type="checkbox"/>

	U	1	D	cument ID	I	su	Date	Pat	Title	Curr nt OR
28	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5061027 A	19911029					Solder-bump attached optical interconnect structure utilizing holographic elements and method of making same	385/14
29	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4866507 A	19890912					Module for packaging semiconductor integrated circuit chips on a base substrate	174/258

	Curr nt	XR f	R tri val	Inv ntor	S	C	P	2	3	4	5
			cla sif								
28	250/227.11; 257/448; 359/15; 359/900; 385/131; 385/37; 398/164			Richard, Fred V.	<input type="checkbox"/>						
29	174/250; 257/659; 257/664; 257/684; 257/700; 257/E23.079; 257/E23.173; 361/748; 361/784			Jacobs, Scott L. et al.	<input type="checkbox"/>						

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		□	
28			□

S a r h T rms	
1	CORR-WILLIAM-E
2	CORR-WILLIAM-E.IN.

	Total	USPAT	US-PGPU	EP	JPO	D rw nt	IBM TDB	USOCR
1	4							
2	3							

	U	1	Docum nt ID	Is ue Dat	Pag s	Title	Curr nt OR
1	<input type="checkbox"/>	US	20030083840	20030501	20	Apparatus and method for determining effect of on-chip noise on signal propagation	702/117
2	<input checked="" type="checkbox"/>	US	20030025712	20030206	42	Interpolation error minimization for data reduction	345/606
3	<input checked="" type="checkbox"/>	US	20020133748	20020919	12	Circuit for measuring on-chip power supply integrity	714/25

	Curr nt XR f	R tri val Classif	Inv ntor	S	C	P	2	3	4	5
1		Corr, William E.		☒	<input type="checkbox"/>					
2		Corr, William E.		<input type="checkbox"/>						
3		Corr, William E.		<input type="checkbox"/>						

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1	US 20030083840	<input type="checkbox"/>
2	US 20030025712	<input type="checkbox"/>
3	US 20020133748	<input type="checkbox"/>